High-Performance Design with Rapid RTL Profiling of Critical Power Scenarios

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Motivation: The challenges from high current events

Peak di/dt events:

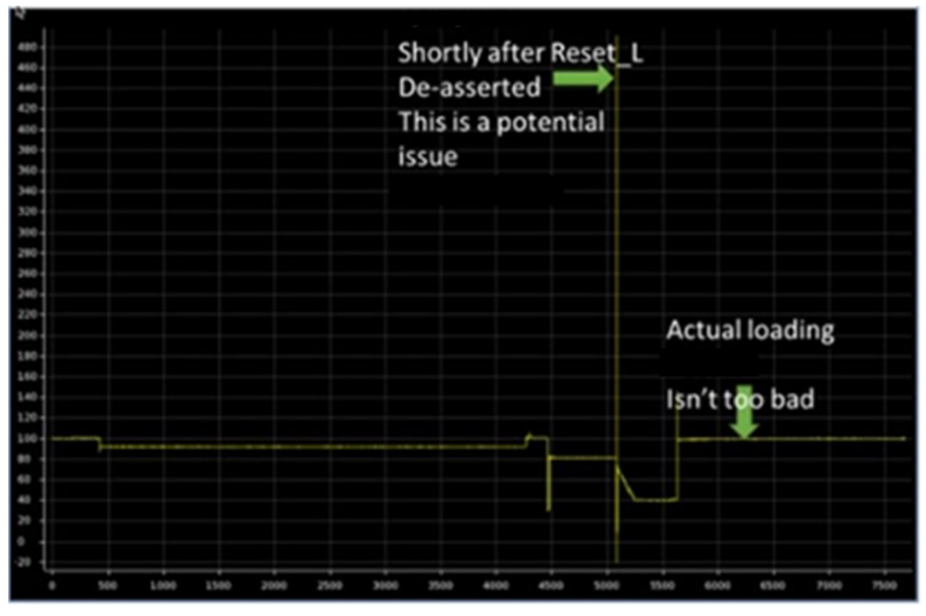
- Peak di/dt events are the result of the sudden high current demand caused by a large number of simultaneous switching activities from the workload
- These large current spikes can happen during application runs for various reasons such as:
  - Multiple clocks start running at a higher frequency that cause a lot of logic to toggle
  - Reset getting de-asserted and causing many logic branches to toggle at the same time

Effects of Peak di/dt events on Power and Performance:

- Unless appropriate mitigation strategies are in place, these di/dt events can cause significant voltage drops in the power grid
- As a result of this voltage drop, the V-F curve can shift, and it can cause higher power dissipation as well as a decrease in FMAX

Design Requirement:

- Need for fast di/dt and peak power cycle detection, early in the flow to avoid identifying issues late in the flow, with coverage across real application scenarios
- However, when the simulation is long, it is not feasible to run traditional cycle-based power as it takes too long to run



Main Idea: RTL stage analysis and mitigation of di/dt

From an analysis of RTL level switching activity profiles of representative workloads and their dynamic power profiles, the critical windows where adverse di/dt events might occur can be revealed

RTL stage solutions for better Power & Performance:

(i) Implement RTL/design fixes to curb excessive switching events

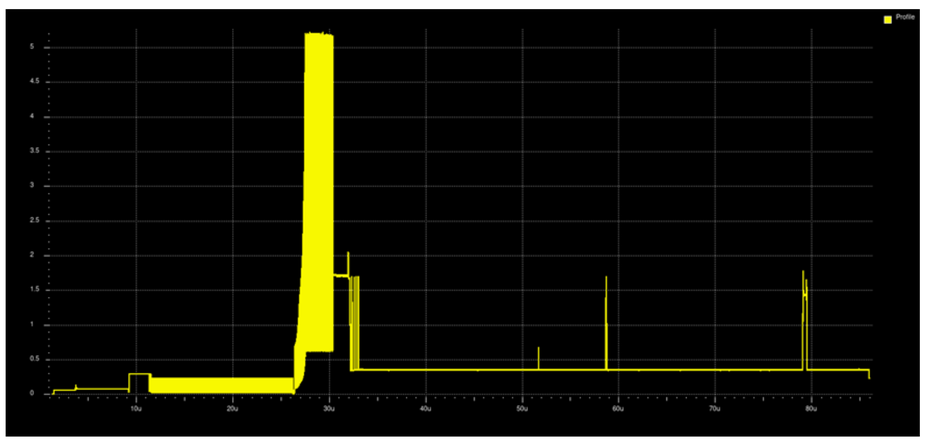
(ii) stagger events to prevent excessive switching on the same critical window

(iii) identify the root cause of excessive activity in a window and implement possible fixes

Key advantages of RTL stage solutions:

(i) Less dependency on expensive layout-level solutions, which translates into significant savings in block/chip area and improvement of power/performance (i.e., reduced layout area implies better timing, improved FMAX)

(ii) Left-shift approach, faster design closure and turnaround time (TAT)



Results generated using Ansys PowerArtist ProfilePower

Use case: RTL FSDB with millisecond duration and <10GB in size

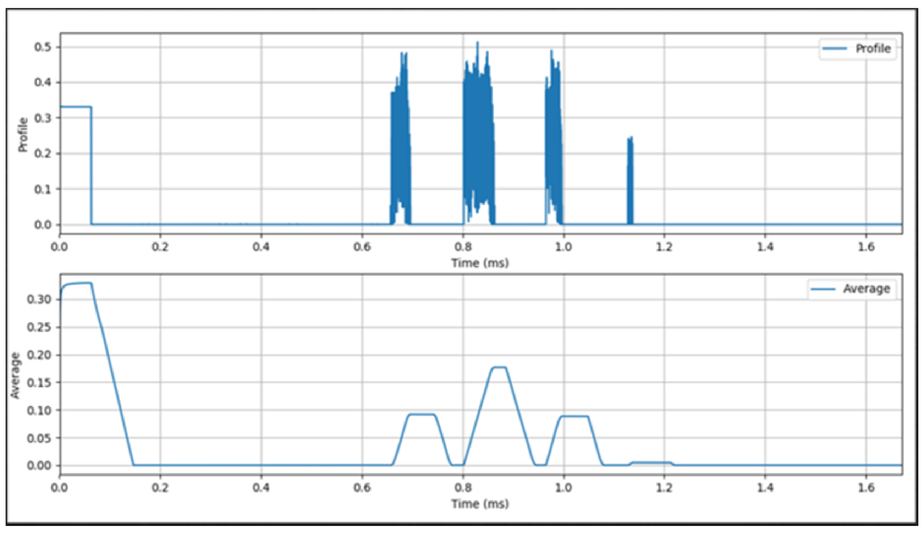
Performance of rapid power profiling: Ran for <4 hours and consumed <60 GB of memory

Design feedback: The power profiling simulation seems to work well

Multi-step Rapid Power Profiling, early at RTL

A multi-step methodology for rapid detection of critical power events:

- Step 1: Use new rapid RTL power profiling simulation to understand when relatively high power is observed. Get a rough assessment of the timing and magnitude of the di/dt event
- Step 2: Run detailed per-cycle power simulation on that small time window to get the exact impact
- Step 3: Higher coverage can be achieved by identifying additional windows in which di/dt is significant within much larger FSDB (s), produced from emulation



Results generated using Ansys PowerArtist ProfilePower

Clock frequency: **MHz range**

VCS simulation duration (FSDB duration): **Several milliseconds**

Activity file size: **>100 GB**

Performance of rapid power profiling: **<4 hours**

Conclusion

Unless appropriate mitigation strategies are in place, di/dt events can cause significant voltage drops in the power grid.

This can cause higher power dissipation as well as a decrease in FMAX.

Analysis of RTL level switching activity profiles of representative workloads and their dynamic power profiles can reveal the critical windows where adverse di/dt events might occur:

- This leads to less dependency on expensive gate level simulations
- Left-shift approach for faster design closure - root cause excessive switching events/activity and implement fixes – achieve high FMAX

Multistep methodology has proven successful with rapid RTL power profiling as the key first step.

- Quick identification of time instances and windows where worst-case di/dt events occur with high fidelity of cycle selection. Runs using Ansys PowerArtist complete within several hours for vectors of several milliseconds in duration, enabling design iterations
- Using this window information, a detailed time-based power run done on those short frames to quantify the di/dt events and explore RTL-stage mitigation methods.